2818

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject:

Serial No. 10/016,898 12/14/01

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HIGHLY-SCALABLE, TWO-TRANSISTOR FLASH EEPROM CELLS, CELL ARRAYS AND PREFERRED OPERATION SCHEMES FOR IN-SYSTEM PROGRAMMABLE LOGIC DEVICE WITH LOGIC DEVICE WITH SIMPLIFIED ON-CHIP STATE-MACHINE

Grp. Art Unit: 2818

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and

Signature/Date _____

U.S. Patent 6,108,239 to Sekariapuram et al., "High-Density Nonvolatile Memory Cell," discusses a compact nonvolatile programmable memory cell which has a substantially transverse or vertical channel relative to the surface of the semiconductor substrate.

U.S. Patent 6,078,521 to Madurawe et al., "Nonvolatile configuration Cells and Cell Arrays," discusses a nonvolatile memory cell directed toward a compact layout and a high logic output voltage.

U.S. Patent 5,914,904 to Sansbury, "Compact Electrically Erasable Memory Cells and Arrays," discloses a nonvolatile memory cell that has a read device, a program device and a tunnel diode.

U.S. Patent 5,904,524 to Smolen, "Method of Making Scalable Tunnel Oxide Window with no Isolation Edges," discloses a device and method directed toward an EEPROM device that has a self aligned tunnel window with low gate capacitance and avoids defects caused by field oxide induced stress in the tunnel oxide.

speed and high density PLD applications.

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U.S. Patent 5,862,082 to Dejenfelt et al., "Two Transistor Flash EEPROM Cell and Method of Operating Same," discusses a device directed toward a flash EEPROM cell that has two transistors with one transistor being a floating gate type device with asymmetric source and drain.

Sincerely,

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